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CHRISTOPHER J. RECKAMP
MARKISON & RECKAMP, P.C.
P. O. BOX 06229
WACKER DRIVE
CHICAGO, IL 606060229

EXAMINER
PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
2673	21

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/287,776	KANG ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 5-10, 12-17, and 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ranganathan (US 5,764,201).

Regarding claim 1, Ranganathan discloses a video overlay apparatus comprising: a video scaler [Fig. 8A; 64] operatively responsive to input video data; and a programmable switching mechanism [Fig. 8A; 68], operatively coupled to the video scaler, to programmably switch video data from the video scaler into one of first and second video overlay generators [Fig. 8A; 32 & 42] that are each capable of being operably coupled to corresponding first and second display devices [Fig. 8B; 22 & 24], in order to enable the display of the video data from the video scaler

and overlay data from one of the first and second overlay generators on one of a first output display device and a second display device (Column 8, Line 18 - Column 10, Line 7).

Regarding claims 2, 10 and 16, Ranganathan discloses the programmable switching mechanism includes a programmable register [Fig. 8A; 67] (Column 9, Lines 37-46).

Regarding claim 3, Ranganathan discloses a first display engine [Fig. 8A; 52] responsive to first graphics data for generating first video window timing data; a second display engine [Fig. 8A; 53] responsive to second graphics data for generating second video window timing data; a first video overlay generator [Fig. 8A; 32] operatively responsive to the first graphics data; and a second video overlay generator [Fig. 8A; 42] operatively responsive to the second graphics data (Column 9, Lines 5-36).

Regarding claims 5 and 19, Ranganathan discloses the programmable switching mechanism includes a selectable video clock source [Fig. 8B; VCLK] operatively coupled to the video scaler wherein the video scaler scales input video corresponding to a display engine for at least one of a plurality of video overlay generators in response to a video clock signal output from the selectable video clock source (Column 8, Line 18 - Column 10, Line 7).

Regarding claims 6, 12 and 20, Ranganathan discloses the programmable switching mechanism further facilitates programming of frame buffer space for each display engine based

on which video overlay generator has been selected to receive input video (Column 12, Lines 4-12).

Regarding claims 7, 13 and 21, Ranganathan discloses the selectable video clock source includes a programmable switch to facilitate switching between a plurality of display dependent clock signals that are selectively coupled to a common video scaler line buffer (Column 4, Lines 7-16).

Regarding claims 8, 14 and 22, Ranganathan discloses a user interface operable to control the programmable switching mechanism to facilitate selective overlay display on a per application basis (Column 8, Lines 57-66).

Regarding claim 9, the limitations were previously addressed in the above rejection of claims 1, 3, 5 and 19.

Regarding claim 15, the limitations were previously addressed in the above rejection of claim1.

Regarding claim 17, the limitations were previously addressed in the above rejection of claim 3, furthermore Ranganathan discloses generating a first video overlay [Fig. 10A & 10B; 22] based on the first graphics data and at least a portion of selectively routed input video data; and generating a second video overlay [Fig. 10A & 10B; 24] based on the second graphics data

and at least a portion of selectively routed input video data (Column 10, Line 60 - Column 11, Line 15).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ranganathan (US 5,764,201) in view of Blahut et al. (US 5,570,126).

Regarding claims 4 and 11, Ranganathan does not expressly disclose operating a graphics data unpacker, a keyer, and a data packer in unison. However, Blahut does disclose a graphics data unpacker [Fig. 4; 418 & 420] operative to unpack graphics data received from a respective display engine [Fig. 4; 410]; a keyer [Fig. 4; 430 & 432] operatively coupled to the graphics data unpacker and responsive to selectively route video data from a programmable switching mechanism [Fig. 4; 440]; and a data packer [Fig. 4; 444] operatively coupled to the keyer to pack combined video and graphics data from the keyer (Column 6, Lines 11-49).

Ranganathan and Blahut are analogous art, because they are from the shared field of video overlay apparatuses. Therefore, it would have been obvious to one skilled in the art at the time of invention to use Blahut's data unpacker / keyer / data packer combination with Ranganathan's video overlay apparatus, so as to maintain overlay operations while processing compressed graphics data.

Regarding claim 18, the limitations were previously addressed in the above rejection of claims 4 and 11, furthermore Blahut discloses keying [Fig. 4; 430, 432, and 440] video and graphics data from a respective display engine [Fig. 4; 410] and the selectively routed video data selectively routed by a programmable switching mechanism [Fig. 4; 440]; and packing [Fig. 4; 444] combined video and graphics data for each respective video graphic overlay generator [Fig. 4; 414 and 416] for alternate output to the display (Column 6, Lines 21-49).

Response to Arguments

5. Applicants' arguments filed 19 May 2003 have been fully considered but they are not persuasive. Firstly, the applicants contend the cited prior art of Ranganathan (US 5,764,201) neglects to disclose a programmable switching mechanism to switch video data into one of first and second video overlay generators. However, the examiner respectfully disagrees. Ranganathan explicitly discloses a programmable switching mechanism [Fig. 8A; 68 working in conjunction with 67] to switch video data [Fig. 8A; output from 52, 53 60, & 68] into one of first and second video overlay generators [Fig. 8A; 32 & 42] (see Column 8, Line 18 - Column 10, Line 7). Ranganathan's multiplexer [Fig. 8A; 68] is inherently a ***programmable switching mechanism***, selectively switching between plural input data signals [Fig. 8A, 64 & 66]. Furthermore, although the applicants are correct in noting that Ranganathan's video overlay generators [Fig. 8A; 32 & 42] are pixel multiplexers; they are incorrect in the assumption that ***pixel muxes*** cannot be construed as ***video overlay generators***. Ranganathan expressly discloses,

"Pixel muxes 32, 42 independently select either ***movie overlay data*** from YUV path 34 or graphics pixels from RGB path 36" (see Column 9, Lines 5-7).

Secondly, the applicants contend Ranganathan fails to teach the generation of first and second video window timing data. The examiner respectfully disagrees. Ranganathan explicitly discloses, "The hardware cursor and icons may be switched in to either or both displays as needed." (see Column 9, Lines 35-36). Moreover, Ranganathan discloses, "FIG. 9 is an alternate embodiment of the dual graphics controller of FIG. 8B which allows for separate refresh rates of the CRT and LCD displays" (see Column 10, Lines 10-12). Furthermore, Ranganathan discloses, "Movie window 28 is overlaid on 'top' of the graphics screen data so that the graphics data underneath movie window 28 is not visible" (see Column 5, Lines 17-46). Still further, Ranganathan teaches, "Two or more movie windows may be separately overlaid onto the graphics data by additional logic, or preferably re-use of the existing logic" (see Column 12, Lines 19-21). Such movie windows inherently have separate and unique timing data from the static graphics data that they overlay, and from each other.

Thirdly, the applicants contend Ranganathan fails to teach the signal VCLK wherein the video scaler scales input video corresponding to a display engine in response to a video clock signal output from the selectable video clock source. The examiner again respectfully disagrees. Ranganathan discloses, "In other aspects a clock generator generates the pixel clock. The clock generator generates a horizontal line clock by dividing the pixel clock. A vertical clock is generated by dividing the horizontal line clock. The vertical clock indicates when a new frame of pixels is to begin. The new frame includes a plurality of horizontal lines signaled by the horizontal line clock" (see Column 4, Lines 6-14). Additionally, Ranganathan recites, "Movie

pixels loaded into movie FIFO 62 are clocked by the video clock to scaler 64 and color-space converter 66" (see Column 8, Lines 57-58).

Fourthly, the applicants contend Ranganathan neglects to teach programming of frame buffer space. The examiner respectfully disagrees. Ranganathan explicitly discloses, "Graphics memory 56 also contains a half-frame buffer 58 which is used to buffer half of the frame being displayed" (see Column 7, Lines 28-29). Ranganathan continues, "A full-frame buffer may be used rather than a half-frame buffer" (see Column 7, Lines 28-29).

Fifthly, the applicants contend Ranganathan fails to teach the selection of clock signals. The examiner respectfully disagrees. As stated previously, Ranganathan discloses, "FIG. 9 is an alternate embodiment of the dual graphics controller of FIG. 8B which allows for separate refresh rates of the CRT and LCD displays" (see Column 10, Lines 10-12). Moreover, Ranganathan teaches, "the pixel data for the movie window is in YUV format rather than RGB format, as is thus stored separately from the RGB graphics data, either in a separate memory, or in a separate part of the frame buffer graphics memory" (see Column 12, Lines 15-19).

Finally, the applicants contend the cited prior art of Blahut et al. (US 5,570,126) neglects to teach unpacking data from a display engine, keying the data unpacker to selectively route data from a data mechanism and a data packer to pack combined video and graphics data from the keyer. However, the examiner respectfully disagrees. Blahut explicitly discloses a graphics data unpacker [Fig. 4; 418 & 420] unpacking (i.e. decompressing) data from a display engine [Fig. 4; 410], a keyer [Fig. 4; 430 & 432] keying the data unpacker to selectively route data from a data mechanism [Fig. 4; 440] and a data packer [Fig. 4; 444] to pack (i.e. compress) combined video and graphics data from the keyer (Column 6, Lines 11-49).

By such reasoning, rejection of the pending claims is deemed proper and thereby maintained at this time.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
August 11, 2003